

PATENT NUMBER

U.S. UTILITY Patent Application

<p>O.I.P.E.</p> <p>SCANNED <u>PD²</u> Q.A. <u>A.G.</u></p>	<p>PATENT DATE</p>
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CLASSIFICATION NO. 09/620649	CONT/PRIOR D	CLASS 438 257	SUBCLASS 316	ART UNIT 2822	EXAMINER W/czewski
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APPLICANTS

Cetin Kaya

3.1.1.1

Integrated circuit having independently formed array and peripheral isolation dielectrics

PTO-2040
1289[illegible]

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg. <i>5</i>	Figs. Drwg. <i>10</i>	Print Fig./ <i>4d</i>	Total Claims <i>1</i>	Print Claim for O.G. <i>1</i>
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) (Date)			NOTICE OF ALLOWANCE MAILED	
	Mary Wilczewski Primary Examiner <i>MW</i> <i>2/2004</i> (Primary Examiner) (Date)			<i>02/11/04</i>	
ISSUE FEE					
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